[0013] FIG. **7** is a simplified plot of trigger voltage Vt**1** of the device of FIG. **6** in volts, as a function of NPN transistor base resistance R_B(NPN) in Ohms;

[0014] FIG. **8** is a simplified plot of the holding voltage Vh of the device of FIG. **6** in volts as a function of the NPN transistor base length L_b(NPN) in micrometers;

[0015] FIG. **9** is a plot of the current (in Amps) versus voltage (in volts) characteristic of the ESD clamps of FIG. **6** with desirable choices of R_B(NPN) and L_b(NPN); and

[0016] FIGS. **10-20** are simplified cross-sectional views of the ESD clamp of FIG. **6** at various stages of manufacture, illustrating a preferred manufacturing process according to still further embodiments of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0017] The following detailed description is merely exemplary in nature and is not intended to limit the invention or the application and uses of the invention. Furthermore, there is no intention to be bound by any expressed or implied theory presented in the preceding technical field, background, or the following detailed description.

[0018] For simplicity and clarity of illustration, the drawing figures illustrate the general manner of construction, and descriptions and details of well-known features and techniques may be omitted to avoid unnecessarily obscuring the invention. Additionally, elements in the drawings figures are not necessarily drawn to scale. For example, the dimensions of some of the elements or regions in the figures may be exaggerated relative to other elements or regions to help improve understanding of embodiments of the invention.

[0019] The terms "first," "second," "third," "fourth" and the like in the description and the claims, if any, may be used for distinguishing between similar elements and not necessarily for describing a particular sequential or chronological order. It is to be understood that the terms so used are interchangeable under appropriate circumstances such that the embodiments of the invention described herein are, for example, capable of operation or manufacture in sequences other than those illustrated or otherwise described herein. Furthermore, the terms "comprise," "include," "have" and any variations thereof, are intended to cover non-exclusive inclusions, such that a process, method, article, or apparatus that comprises a list of elements is not necessarily limited to those elements, but may include other elements not expressly listed or inherent to such process, method, article, or apparatus. The term "coupled," as used herein, is defined as directly or indirectly connected in an electrical or non-electrical manner.

[0020] While the arrangements of FIGS. **2** and **3** can be effective in providing ESD protection, further improvements are desirable. As noted above, there is an ongoing need to provide improved ESD clamps, especially ESD clamps that are immune to rapid signal transients, especially in high speed devices and ICs fabricated in deep sub-micron technologies. Other desirable features and characteristics of the present invention will become apparent from the subsequent detailed description of the invention and the appended claims, taken in conjunction with the accompanying drawings and this description of the invention. For convenience of explanation, various embodiment of the ESD clamps of the present invention are described for particular combinations of N and P type doping providing, for example, NPN bipolar transistors and PNP bipolar transistors, but persons of skill in the art will understand that this is not intended to be limiting and that opposite types of devices may be provided by interchanging the doping types, wherein a PWELL is substituted for an NWELL, a P type buried layer (PBL) for an N type buried layer (NBL), a P+ contact, source, drain, emitter or collector for an N+ contact, source, drain, emitter or collector, and vice-versa. Thus, the identification of various regions as being either P or N type is merely for convenience of description and that, more generally, such regions may be identified as being of a first conductivity type that is either P or N type or of a second, opposite, conductivity type that is accordingly N or P type.

[0021] It has been found, that the false ESD clamp turn-on associated with fast operating signal events appearing on I/O **22** can be avoided by using ESD protection based on bipolar transistors instead of MOS transistors. Furthermore, for reliability purpose, it is highly desirable to separately optimize the trigger voltage Vt**1** and the holding voltage Vh, so that the trigger voltage Vt**1** can be lower than the degradation (ESD transient) voltage of the core circuit and the holding voltage can be higher than the operating voltage of the core circuit. Ideally, when the operating voltage and the degradation voltage are close, the ESD protection should have as little snapback as possible, that is, it is desirable to have Vh~Vt**1**. FIG. **5** is a simplified combined cross-sectional and electrical schematic diagram illustrating generalized ESD clamp **60** according to an embodiment of the present invention. Clamp **60** comprises substrate **61** having upper surface **612**, PWELL **62** of depth **621** from surface **612** and abutting or proximate NWELL **64** of depth **641** from surface **612** and with PN junction **65** therebetween. Substrate **61** may be either N or P type or comprise a dielectric with semiconductor **61** thereon, as for example and not intended to be limiting, in a semiconductor-on-insulator (SOI) structure. In various other embodiments, the conductivity types of wells **62**, **64** of FIG. **5** and wells **82**, **84** of FIG. **6** may be interchanged and as used herein the designation "PN" referring, for example, to junction **65** and other junctions is intended to include such variations. Located in PWELL **62** is P+ region **66** and N+ region **67** extending from surface **612**. Located in NWELL **64** is P+ region **68** and N+ region **69** extending from surface **612**. P+ regions **66**, **68** have depth **662** from surface **612** and N+ regions **67**, **69** have depth **672** from surface **612**. Doped regions **66**, **67**, **68**, **69** have conductive (e.g., metal or silicide) contacts **661**, **671**, **681**, **691** respectively. N+ (emitter) region **67**, PWELL (base) **62** with P+ base contact region **66** and NWELL (collector) **64** with N+ collector contact region **69** form lateral NPN transistor **70** with lateral base width L_b(NPN) **74**. P+ (emitter) region **68**, NWELL (base) **64** with N+ base contact region **69** and PWELL (collector) **62** with P+ collector contact region **66** form lateral PNP transistor **72** with lateral base width L_b(PNP) **76**. Base resistor R_b(NPN) **78** is coupled between contact **671** of N+ emitter region **67** and contact **661** of P+ base contact region **66** of lateral NPN transistor **70**. Base resistor R_b(PNP) **79** is coupled between contact **681** of P+ emitter region **68** and contact **691** of N+ base contact region **69** of lateral PNP transistor **72**. It has been found that by suitably adjusting base resistors **78**, **79** and base widths **74**, **76**, that Vt**1** and Vh can be separately controlled. In particular Vt**1** can be reduced and Vh can be increased, so that Vh and Vt**1** are close or substantially equal, so that ESD clamp **60** operates very reliably.

[0022] FIG. **6** is a simplified combined cross-section and electrical schematic diagram similar to FIG. **5** of ESD clamp **80** according to a further embodiment of the present invention and showing additional details. Clamp **80** comprises substrate **78** (that may be either N or P type or an SOI structure), N type buried layer (NBL) **79** and P-EPI layer **81** of thickness **811** having upper surface **812**. PWELL **82** extends into P-EPI layer **81** to depth **821** from surface **812**. Abutting or proximate NWELL **84** extends into P-EPI layer **81** to depth **841** from surface **812** and forms PN junction **85** with PWELL **82** or any